Please amend the paragraph on page 1, lines 17-25 as follows:

A2

Conventionally, BGA packages are fabricated in batch on a substrate strip composed of a series of substrates. One problem of the conventional substrate strip structure, however, is that each substrate thereon would easily suffer from thermally-stressed warpage during high-temperature fabrication steps, such as during die-bond cure, wire bonding, molding, and molding cure, during which the temperature is typically about 200°C. The warped substrate would then cause an uncoplanarity problem to the subsequently implanted solder balls on the back side thereof, which would adversely affect the quality of the subsequent mounting of the BGA packages on external printed circuit boards (PCB). This thermally-stressed warpage problem is illustratively depicted in the following with reference to FIGs. 1A-1D.

Please amend the paragraph on page 2, lines 1-8 as follows:

A3

FIG. 1A is a schematic diagram showing a sectional view of a typical BGA package. As shown, the BGA package is constructed on a substrate 11 whose front side 11a is mounted with a semiconductor chip 20 and whose back side 11b is implanted with a grid array of solder balls (i.e., ball grid array) 30. The semiconductor chip 20 can be electrically coupled to the substrate 11 by means of the well-known wire-bonding technology or flip-chip technology. During a subsequent SMT (Surface Mount Technology) process, the BGA package can be mechanically bonded and electrically coupled to an external printed circuit board (PCB) 40 by means of the ball grid array 30.

Please amend the paragraph on page 2, lines 9-17 as follows:

A4

Referring further to FIG. 1B, in fact, BGA fabrication is typically implemented in batch on a substrate strip 10 which is composed of a series of substrates 11 supported on a frame 12 having a pair of parallel elongated supporting bars 12a, 12b. Each of the substrates 11 is used for the fabrication of an

Cond A4

individual unit of a BGA package. Conventionally, each of the substrates 11 is rectangularly-shaped and linked to the supporting bars 12a, 12b by means of a four-point linkage structure consisting of four tie bars 13a, 13b, 13c, 13d on the four corners thereof. Typically, the upper-left tie bar 13a is also used to provide a gate (not shown) which is used for the injection of encapsulant during the fabrication of an encapsulation body (not shown) for encapsulating the semiconductor chip 20.

Please amend the paragraph on page 3, lines 1-5 as follows:

A5

As further shown in FIG. 1D, when the thermally-warped substrate 11 is implanted with the ball grid array 30, it would cause the implanted ball grid array 30 to have poor coplanarity. During the subsequent SMT process, this BGA uncoplanarity would cause some solder balls in the ball grid array 30 to be unreliably bonded to the PCB 40, thus resulting in a reliability problem in the BGA package.

Please amend the paragraph on page 3, lines 15-23 as follows:

A6

The U.S. Patent No. 5,652,185 discloses an inventive method of packaging a BGA assembly with a substrate that has been formed from a substrate strip whose area has been maximized. The U.S. Patent No. 5,635,671 discloses a package assembly constructed on a substrate with a novel degating region to allow removal of excess encapsulant formed on the substrate surface during molding without damaging the remainder of the device. The U.S. Patent No. 5,691,242 discloses an advanced method for packaging an integrated circuit on an organic substrate. All of these patents, however, utilize a substrate strip with the above-mentioned four-point linkage structure, so that the above-mentioned warpage problem during high-temperature fabrication steps still exists.

Please amend the paragraph on page 4, lines 5-12 as follows:

A7

The substrate strip of the invention is characterized by the provision of a warpage-preventive linkage structure, by which each substrate on the substrate strip is supported by means of no more than two tie bars, i.e., either by a two-point linkage structure or a one-point linkage